

Appl. No. 10/707,261
Amdt. dated November 19, 2004
Reply to Office action of October 19, 2004

Amendments to the Claims:

1. (Currently amended) A method for fabricating a trench capacitor, comprising:
- 5 providing a substrate having thereon a pad oxide layer and a pad nitride layer;
etching in order of said pad nitride layer, said pad oxide layer, and said substrate to
form a deep trench;
doping said deep trench to form a buried diffusion plate in said substrate at a lower
portion of said deep trench;
- 10 lining said deep trench with a node dielectric layer;
performing a first polysilicon deposition and recess etching to embed a first
polysilicon layer on said node dielectric layer at said lower portion of said deep trench,
and said first polysilicon layer having a top surface, wherein said top surface of said first
polysilicon layer and sidewall of said deep trench define a first recess;
- 15 forming a collar oxide layer on sidewall of said first recess;
performing a second polysilicon deposition and recess etching to embed a second
polysilicon layer on said first polysilicon layer;
removing said collar oxide layer that is not covered by said second polysilicon layer
to expose said substrate at an upper portion of said deep trench, and wherein a top surface
- 20 of said second polysilicon layer and said exposed substrate define a second recess;
filling said second recess with a spacer material layer;
forming a photoresist layer on said spacer material layer, and said photoresist layer
masking a portion of said spacer material layer;
anisotropically etching said spacer material layer not covered by said photoresist
- 25 layer, to form a single-sided spacer on the sidewall of said second recess; and
performing a third polysilicon deposition and recess etching to embed a third
polysilicon layer on said second polysilicon layer and said collar oxide layer, wherein
dopants of said third polysilicon layer diffuse out to the surrounding substrate that is not

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masked by said single-sided spacer to form a non-annular buried strap out diffusion.

2. (Original) The method of claim 1 wherein said substrate is a silicon substrate.
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3. (Original) The method of claim 1 wherein said deep trench has a depth that is larger than 6 microns below a surface of said substrate.
4. (Original) The method of claim 1 wherein doping said deep trench to form a buried diffusion plate in said substrate involves the use of an arsenic silicate glass (ASG) film.
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5. (Original) The method of claim 1 wherein said node dielectric is an oxide-nitride-oxide (ONO) dielectric layer.
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6. (Original) The method of claim 1 wherein said spacer material layer is silicon dioxide.
7. (Original) The method of claim 6 wherein said silicon dioxide is formed by chemical vapor deposition (CVD) method.
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8. (Currently amended) A method for fabricating a trench capacitor, comprising:
providing a substrate having thereon a pad oxide layer and a pad nitride layer;
etching in order of said pad nitride layer, said pad oxide layer, and said substrate to form a deep trench;
25 doping said deep trench to form a buried diffusion plate in said substrate at a lower portion of said deep trench;
lining said deep trench with a node dielectric layer;
performing a first polysilicon deposition and recess etching to embed a first polysilicon layer on said node dielectric layer at said lower portion of said deep trench,

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and said first polysilicon layer having a top surface, wherein said top surface of said first polysilicon layer and sidewall of said deep trench define a first recess;

forming a collar oxide layer on sidewall of said first recess;

5 performing a second polysilicon deposition and recess etching to embed a second polysilicon layer on said first polysilicon layer;

removing said collar oxide layer that is not covered by said second polysilicon layer to expose said substrate at an upper portion of said deep trench, and wherein a top surface of said second polysilicon layer and said exposed substrate define a second recess;

10 forming a single-sided spacer on sidewall of said second recess; and

performing a third polysilicon deposition and recess etching to embed a third polysilicon layer on said second polysilicon layer and said collar oxide layer, wherein dopants of said third polysilicon layer diffuse out to the surrounding substrate that is not masked by said single-sided spacer to form a non-annular buried strap out diffusion.

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9. (Original) The method of claim 8 wherein said single-sided spacer is made of silicon dioxide.

10. (Original) The method of claim 8 wherein said single-sided spacer is used to isolate
20 a portion of said third polysilicon layer from said substrate.